

Appln No. 09/592,009

Amdt date May 9, 2005

Reply to Office action of February 9, 2005

Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently Amended) A method of performing a context switch operation, comprising ~~the acts of:~~

accessing context data in a first register of a peripheral system, ~~the first register being associated with~~ when a context index is set to a first index value;

receiving, by the peripheral system, a second index value from a host computer associated with the peripheral system;

setting the context index to the second index value to perform a context switch;

accessing context data in a second register of the peripheral system, ~~the second register being associated with~~ when the context index is set to the second index value.

2. (Original) The method recited in claim 1, wherein context data further includes:

a device address for one of a plurality of network devices;

a class value;

a clock offset value; and

an active member address.

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3. (Currently Amended) The method recited in claim 1, wherein the accessing context data in a second register further comprises:

receiving, by the peripheral system, an address value that identifies an address within the second register;

receiving, by the peripheral system, a control input that identifies at least one of a plurality of functions, the plurality of functions including a read function and a write function;

receiving, by the peripheral system if the control input identifies the write function, a data value; and

if the control input identifies the write function, writing the data value to the second register at the address identified by the address value.

4. (Currently Amended) The method recited in claim 1, wherein the accessing context data in a second register further comprises:

receiving, by the peripheral system, an address value that identifies an address within the second register;

receiving, by the peripheral system, a read control input; and

providing the contents of the second register at the address identified by the address value to the host computer.

5. (Currently Amended) The method recited in claim 1, wherein the accessing context data in a second register further comprises:

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receiving, by the peripheral system, an address value that identifies an address within the second register;

receiving, by the peripheral system, a data value;

receiving, by the peripheral system, a write control input;

and

writing the data value to the second register at the address identified by the address value.

6. (Currently Amended) The method recited in claim 1, wherein the accessing context data further comprises:

receiving, by the peripheral system, an address value that identifies an address within the second register;

receiving, by the peripheral system, a control input that identifies one of a plurality of functions, the plurality of functions including a read function and a write function; and

if the control input identifies the read function, providing the contents of the second register at the address identified by the address value to the host computer.

7. (Original) The method recited in claim 1, wherein the first and second registers are not architected registers.

8. (Original) A system, comprising:

a host computer, the host computer including a microprocessor;

at least one peripheral system coupled to the host processor, the peripheral system including a first register, the first register being associated with a first index value, the

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peripheral system further including a second register, the second register being associated with a second index value;

an interface coupled to the host computer and to the peripheral system, the interface being configured to provide the first and second index values from the host computer to the peripheral system; and

a register access circuit coupled to the host computer, the register access circuit being configured to access the first register if the first index value is provided by the host computer, the register access circuit being further configured to access the second register if the second index value is provided by the host computer.

9. (Currently Amended) The system recited in claim 8, wherein the first and second ~~context~~ registers are not architected registers.

10. (Original) The system recited in claim 8, wherein the peripheral system includes a state machine module, the state machine module including:

an address portion;

a control portion; and

a data portion, the first register and the second register being included in the data portion.

11. (Original) The system recited in claim 8, wherein the peripheral system includes a microprocessor.

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12. (Currently Amended) The system recited in claim 10, wherein the address portion comprises [[a]] the register access circuit.

13. (Currently Amended) The system recited in claim 8, wherein the peripheral system includes a plurality of context registers, wherein each of the plurality of context registers is associated with one of a plurality of index values other than the first and second index values.

14. (Currently Amended) The system recited in claim 8, wherein the peripheral system includes at least one index register for storing the first and second index values.